16. The system of claim **14**, wherein to determine the number of pulses received during the predetermined period of time, the first integrated circuit is further configured to increment a counter in response to detecting a particular pulse of the plurality of pulses received during the predetermined period of time.

17. The system of claim **16**, wherein the first integrated circuit is further configured to reset the counter in response to a determination that the predetermined period of time has elapsed.

18. The system of claim **16**, wherein the counter includes a plurality of flip-flop circuits, wherein each flip-flop circuit of the plurality of flip-flop circuits is coupled to a clock signal included in the first integrated circuit.

19. The system of claim **14**, wherein the predetermined period of time is programmable.

20. The system of claim **14**, wherein the first integrated circuit is further configured to adjust at least one performance parameter dependent upon the value of the average current through the inductor.

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